Reliability Metrics considered in the realm of Digital Systems and Bit-Cell Memory

Lance Madarang
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2362

***Abstract*—The first object of this paper is to program a method of counting the number of times the word inputted appears with the given statement as well as the indexes where the word occurred in the string statement. The energy consumption that generates the least is the DNU-latch memory system which yields around 38,000fJ. The second is to describe the reliability metrics used when dealing with faulty errors that occurs with a circuit, transistor, or etc. Such reliability constraints include the integrity of the components of the circuits, power consumption and how to detect and fix the errors that might occur. One of the most effective method of searching for faulty errors is the Triple Modular Redundancy (TMR) where if one input is incorrect and the other two inputs are correct, the system can "mask" the error and give the correct output.**

Keywords—Triple Modular Redundancy (TMR), radiation hardening process, single-event upset (SEU), single-event upset tolerance Dual interchange-storage cell latch, Double node upset (DNU)

I. INTRODUCTION

A. Project Design

The objective of the MIPS assembly code was to construct a program which will allow the user to input two words that are within ten letter characters only and search them with the given statement. Then the output will display how many times the two words are displayed in that statement as well as the indexes of when those words occurred. A potential theory of calculating the amount of appearances of the given words was to convert the words and the statement itself to lowercase so that there would be no complications of characters. Then, to compare the word with the statement, a program is set up where the code searches the letters individually, if the statement and word completely match, then a counter would be set and repeat the process until the statement array hits a null character. As for the indexes, a solution would be to create two index arrays where if the initial condition where both the statement and the index are identical, then an index register would store the first letter of the specified word and hold its index number in the statement string and another register would count that index. For the index output, there would be a "for loop" statement where the index counter will iterate the stored index occurrences and print them out.

B. Test Cases

For the output, the test inputs that were used within the project was "UcF and KNight" which was used to test whether the program matched the sample result provided. The second test input "tuition and UCF." Will test the condition where the input has to be formatted in all letter characters and special characters would yield nothing. Looking that "UCF." There should not have any occurrences or appearances as the program does not include any special characters in the input. Lastly, the test code "information and the" will test whether the character limit is 10. The word input for information will cut after "informati" due to the max character count of 10 and will continue on for the second word input.

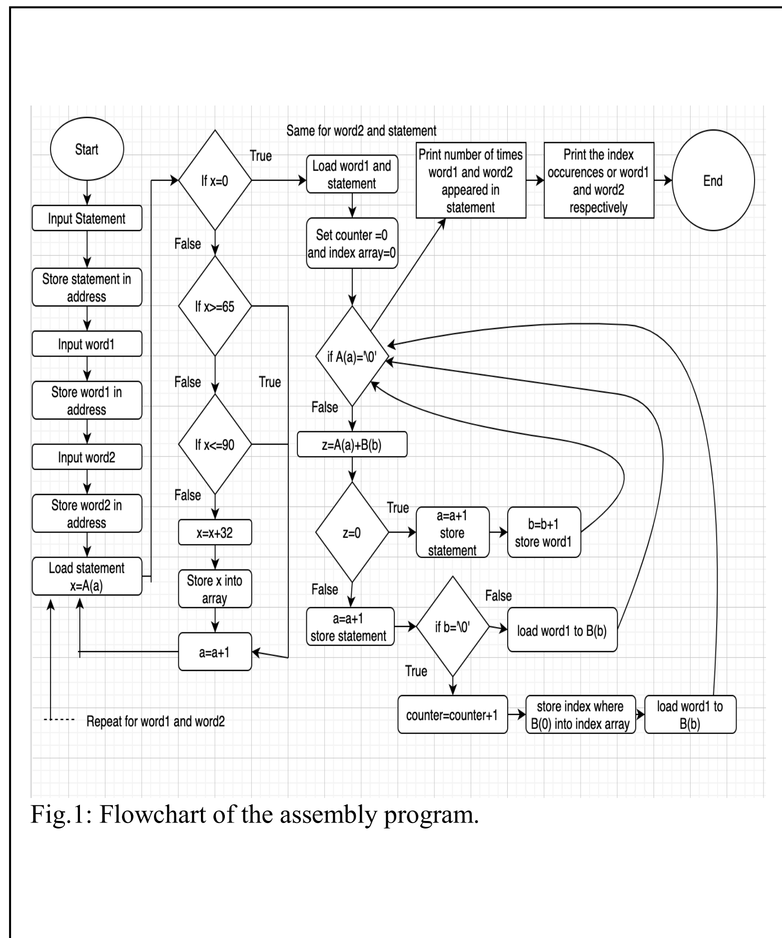

Fig.1: Flowchart of the assembly program.

```
#Please type the first word (up to 10 characters) that you are looking for:UcF

#Please type the second word (up to 10 characters) that you are looking for:KNight

#Number of times the word ucf
was found in the input statement: 2

#Number of indexes found:

#Number of times the word knight
was found in the input statement: 6

#Number of indexes found:
-- program is finished running --

#Please type the first word (up to 10 characters) that you are looking for:Tuition

#Please type the second word (up to 10 characters) that you are looking for:UCF.

#Number of times the word tuition
was found in the input statement: 1

#Number of indexes found:

#Number of times the word ucf.
was found in the input statement: 0

#Number of indexes found:
-- program is finished running --

#Please type the first word (up to 10 characters) that you are looking for:informati

#Please type the second word (up to 10 characters) that you are looking for:the

#Number of times the word informatiwas found in the input statement: 0

#Number of indexes found:

#Number of times the word the
was found in the input statement: 15

#Number of indexes found:
-- program is finished running --
```

Fig.2: Sample outputs of the program.

II. RELIABILITY BIT-CELLS

In the realm of digital systems design, reliability has been an essential factor to consider as failure of a product would lead to financial issues and ineffective products for consumer use. The rise of nanotechnology drastically improves on memory storage performance in circuit design; however, nanotech is extremely delicate and susceptible to error. Present reliability agendas include memory space, energy consumption of a system, any potential damage to components by external means or searching for errors. Examples include the use of radiation hardening process of improving the integrity of electronic component's resistance to high levels of ionization or electromagnetic radiation which could cause noise resulting in inaccuracies.[1] Another reliability factor is to consider single-event upset (SEU) is a process where excited particles in certain areas or nodes that change the internal voltage which leads to data memory loss and issues with the transistors involved. Power consumption is crucial in a systems efficiency as more power being consumed would lead to expensive scenarios exceeding the project budget and the electronic components to overheat breaking the integrity of the circuit design. To find these reliability factors, there should be a method to check the concerns and execute a countermeasure to fix or identify faulty errors.

Triple Modular Redundancy (TMR) is a searching method of fault tolerance in which three different input systems are connected to a majority voter system which will determine the output of the overall system.[4] If an error has occurred in one of the systems, then the other two systems would "mask" that error and the output would not be affected. Although the TMR method can essentially ignore a single faulty error in the system, the user has to consider the time delays of each system accordingly to avoid inconsistent outputs for the voter. For instance, if the time delay of one system is 2.5ns and the other is 1.8ns, there a huge margin of error within the time interval and would output incorrect outputs for the voter which would fail the overall system[6]. Another tradeoff to consider would be the amount of energy being consumed with each of the system and how this could affect the spacing inside the system. However, the biggest concern would be the single point of failure which would be the majority voter system itself. If there are two or all systems that are faulty, it would be difficult for the voter system to correct these errors and would jeopardize the circuit. One possible solution to this would be to cascade another TMR which would effectively reduce the amount of error by rechecking the output values of the first voter system and repeating the process all over again. The tradeoff for this solution would be the complexity of the circuit design and the increased time delay that would slow down the overall circuit design.

III. RESULTS AND DISCUSSION

To find the total energy consumed by the MIPS program, the program will ask for two inputs (ucf and The) and after connecting the MIPS instruction statistics into the MIPS program itself, the instruction statistics will yield the ALU, branch, jump, memory and other instructions to give the total energy required(ALU-12304, branch-2417, jump-8379, memory-4036 and other-26 instruction). After calculating the design specifications, the DNU-Latch has the lowest energy consumption and the most efficient. The DNU latch consists of two single event upset tolerant Dual interchange-storage cell latch (SEU-DICE) which reduces latching delay which increases applications speed at a cost for power consumption and area overhead due to complexity of the circuit design.[5]

1) *ALU = 1 fJ*
2) *Branch = 3 fJ*
3) *Jump = 2 fJ*
4) *Memory = Refer to Table I*
5) *Other=5fJ*

Table I: Energy consumption for a single bit-cell memory in the designs provided in [1-3].

Design	Energy consumption of a Single Bit-Cell Memory
SEU-Latch [1]	0.88 fJ
DNU-Latch [1]	0.28 fJ
[2]	6.96 fJ
[3]	1.51 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
SEU-Latch [1]	40018.4fJ
DNU-Latch [1]	37580.6fJ
[2]	64721.5fJ
[3]	42578.1fJ

IV. Conclusion

One of the agendas discussed in this project is reliability metrics such as power consumption, integrity of the components, and how can a system regulate fault tolerance. One example of system regulation is the Triple Modular Redundancy where three inputs decides the output for the majority voting system. If one of the inputs has an error while the other inputs has the correct inputs, then the system can ignore that faulty error and output the proper value. The other agenda includes the program where a user inputs two words which is less than ten characters and the program will search those words from the hard-coded statement. Then, the program will output the number of times the words appeared in the statement as well as the indexes where they have occurred. As for the energy consumption design specifications, the DNU-Latch proved to be the most efficient.

1) *Knowledge of Triple Modular Redundancy and its applications and tradeoffs*
2) *Learned the concepts of SEU and DNU Latch for a single bit cell memory*
3) *Optimizing an array in MIPS instructions for finding the indexes of the words*
4) *Calculate the energy consumption of the MIPS program*
5) *Developled an understanding of IEEE formatted capstone research papers*

References

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[2] H. Pourmeidani and M. Habibi, "Hierarchical defect tolerance technique for NRAM repairing with range matching CAM," 2013 21st Iranian Conference on Electrical Engineering (ICEE), Mashhad, 2013, pp. 1-6.

[3] K. Katsarou and Y. Tsiatouhas, "Double node charge sharing SEU tolerant latch design," 2014 IEEE 20th International On-Line Testing Symposium (IOLTS), Platja d'Aro, Girona, 2014, pp. 122-127.

[4] R. Hentschke, F. Marques, F.Lima, L Carro, A. Susin and R. Reis "Analyzing Area and Performance Penalty of Protecting Different Digital Modules with Hamming Code and Triple Modular redundancy," Proceedings. 15th Symposium on Integrated Circuits and Systems Design, Porto Alegre, Brazil, 2002, pp. 95-100

This paper focuses on testing the two faulty error analysis, Hamming code and Triple Modular Redundancy in VHDL. Hamming code detects single-bit or double bit errors from a parity bit when there is an odd number of bits that are faulty. This paper concludes that the TMR is efficient in register application, and delay reduction, whereas Hamming code is efficient in register files and memory.

[5] T. Arifeen, A.S. Hassan, J.-A Lee. "A Fault Tolerant Voter for Approximate Triple Modular Redundancy." Electronics 2019,8,332

The paper improves upon the concept of TMR by discussing a scenario of cascading TMR and focusing more on fault tolerance of the voter input after the TMR finishes its part. The authors introduce the principle of Approximate TMR where the circuit design consists of pass transistors and quadded transistor redundancy to increase "masking" faults within the system and overcome area overhead issues.

[6] R. A. Ashraf, A. Alzahrani, R. F. Demara, "Extending Modular Redundancy to NTV: Costs and Limits of Resiliency at Reduced Supply Voltage" Workshop On Near-Threshold Computing (WNTC), 2014

This paper discusses the idea of implementing Near Threshold voltage (NTV) which reduces energy consumption will increases application delay slightly into an N Modular Redundancy (NMR). They tested the frequency and variations for N orders in the NMR systems to test the reliability, delay and integrity of the circuit design.