Optimization of Memory Bit-cells via Self-timed Logic Designs

Fernando Oviedo
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, FL 32816-2362

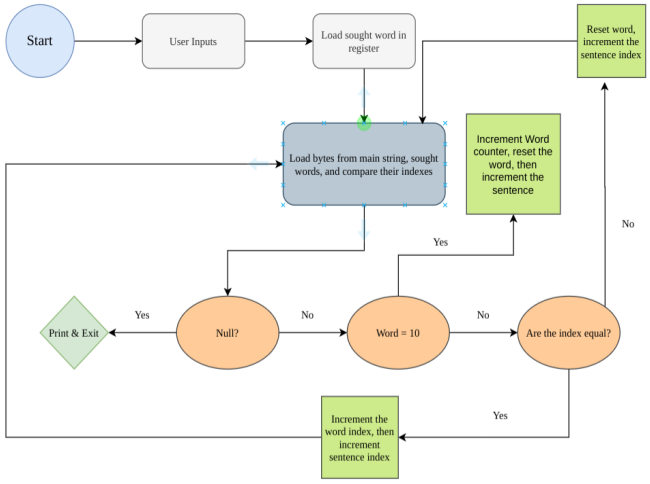
***Abstract*—When using a program that specifically targets a set amount of words, it's important to be mindful of memory leakage and a proper up-counter. With features such as Heterogeneous Configurable Fabrics (HTCF) and Storage Cell Replacement Fabrics (SRCF), it will have a reduction in reconfiguration energy and a higher clock frequency. Also, by adding a Threshold Combinational Reduction (TCR) self-timed logic design versus NULL Conventional Logic (NCL), it allows the user to input a set of words and locate UCF and Knights and place a counter. While the code is designed to ignore the remaining words, it places an index on where to find the selected words throughout the program. Thus, reduction of energy and memory leakage.**

Keywords—HTCF, SRCF, up-counter, TCR, NCL, self-timed logic design.

I. Introduction

The program starts by taking two strings and storing them in a separate location, temporarily. An array is formed from one of the strings to act as a comparison array for the other string. Then the program will compare both strings, looking for similarity hits through loops. Once a similarity is found, the program records both its location and occurrence and stores it in a different register. Once similarities are not found, the program will print the registers in charge of storing the results. The assembly program used in this project takes input1 string from the user and stored into an arbitrary register. An additional input2 string is taken and stored at another register.

The program should find both the location index and occurrence of input2 in input1. This is done through an array formed from input1. The sought input2 will also be automatically formatted to the same format as input1 before being compared to the array of input1. The output will be both the number occurrences and indexes of input2 with input1's array.




```
#Please type in your input statement:
The Knights Graduation and Grant Initiative is a UCF award to help undergraduate
#Please type in the first word (up to 10 characters) that you are looking for (e.g. Knights or KnIGhTs,
#Please type in the second word (up to 10 characters) that you are looking for (e.g. Ucf or uCf, ucf,..
#Number of times the word 'KnIghts' was found in the input statement: 4
#Number of times the word 'UCf' was found in the input statement: 1
```

A. *Project Design*

The flowchart in Fig. 1 gives a general thought of the code's capacity. In the .data area string put away and used to

check the event tally of the user input. In one loop assumes responsibility for stacking bytes from both the predetermined word and the fundamental string, at that point contrasts the predefined word's record and that of the principal string. The primary string's file experiences adjustments to analyze for both lower and capitalized to look for words. In the event that no matches happen in the lists, the looked for word is reset. Be that as it may, if all records in the looked for word coordinates the primary string file, a counter is refreshed. This continues happening and the looked for word is reset ceaselessly until the circle arrives at an invalid end (null) in the fundamental string.

B. Test Cases

As appeared in Fig. 2 three information tests were picked: KniGhts, UcF, and KNIGHTS. Despite the mix of both lower and capitalized words, the projects consider for the word an entirety. Also, the included yields are appeared in Fig. 2 also.

II. Memory Bit-Cells

By dealing with memory-bit cells, a number of factors has to be considered. For instance, the combination of a Range Matching Content-Addressable Memory (RM-CAM) and Triple Modular Redundancy (TMR) has the ability to repair defects at a high error rate with minimal resources [3]. The drive strength of a memory-bit cell is essential because it dictates the overall performance of the memory read, which providing a P-type FET as a read-assist circuit is crucial for this matter to occur[5]. However, in some cases, certain components are not provided. Thus, by applying two separate inverters, one by the input and another by the output, a dynamic latch comparator is created. Which is used for low input offset voltage and high output load drivability; in other words, an increase of drive strength[4].

To have memory-bit cells functioning at optimal level, the energy, power, and frequency has to be taken into account. Several features like Heterogeneous Technology Configurable Fabrics and Storage Cell Replacement Fabrics working together makes it more cost effective, offers more reduction in read energy and high clock frequency than a post CMOS approach[1]. Similarly, the Threshold Combinational Reduction (TCR) requires less transistors, it's faster, reduced critical path delays while creating a carry and a sum to a Full Adder, time, space and power optimized is better than a more conventional canonical design such as NULL Conventional Logic (NCL)[2]. Finally, the newer regime and methods proves to be faster, flexible, more cost effective, and overall better performance than a more conventional method.

III. Results and Discussion

Calculation obtained through:

Energy = (ALU*Table1[ ])+(Jump*3pJ)+(Branch*4pJ)+(Memory*50pJ)+(Other*6pJ)

Table I: Energy consumption for a single bit-cell read operation in the designs provided in [1-5].

Design	Energy Consumption For Each Bit-cell`s Read Operation
[1]	0.37 fJ
[2]	47.09 fJ
[3]	6.96 fJ
[4]	37.6 fJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-5].

Design	Total Energy Consumption
[1]	9.76 fJ
[2]	9.32 fJ
[3]	8.59 fJ
[4]	9.91 fJ

IV. Conclusion

As stated in the analysis, memory-bit cells have multiple components in which all have to be addressed to operate at the highest level. From reducing reconfiguration energy, higher clock frequency, and read energy to fewer gate delays and faster drivability. All components that are needed to provide maximum performance on the memory read functions. Having said all that, the leading energy is the Dynamic Latched Comparator. Due to having a regenerative latch stage, a bigger output drive with the same area and less delays than a more conventional component like the double tail latch, makes it more powerful than the rest of the other options.

References

1. R. F. DeMara, A. Roohi, R. Zand, and S. D. Pyle, “Heterogeneous technology configurable fabrics for field-programmable co-design of cmos and spin-based devices,”

in the 2017 IEEE International Conference on Rebooting Computing (ICRC), pp. 1-4, November 2017.
2. S. C. Smith, R. F. DeMara, J. S. Yuan, D. Ferguson, and D. Lamb, “Optimization of NULL convention self-timed circuits,” Integration, The VLSI Journal, vol. 37, no. 3, pp. 135-165, 2004.
3. H. Pourmeidani and M. Habibi, “Hierarchical defect tolerance technique for NRAM repairing with range matching CAM,” in the 21st Iranian Conference on Electrical Engineering (ICEE), pp. 1-6, May 2013.
4. H. Jeon and Y. B. Kim, “A low-offset high-speed double-tail dual-rail dynamic latched comparator,” in Proceedings of the 20th symposium on Great lakes symposium on VLSI, pp. 45-48, May 2010.
5. Atallah, Francois Ibrahim, et al. “Read-Assist Circuits for Memory Bit Cells Employing a P-Type Field-Effect Transistor (PFET) Read Port(s), and Related Memory Systems and Methods.” Google Patents, Google, 22 Aug. 2017, patents.google.com/patent/US9741452B2/en.