Energy Consumption of Various Memory Cell Technologies During MIPS Code Execution

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Abstract- The purpose of this paper, “Energy Consumption of Various Memory Cell Technologies During MIPS Code Execution”, is to show the efficiency of cutting-edge memory technologies. Some of the main performance metrics of memory technology are read/write speed, energy consumption, and data density. In the modern world efficiency is playing a more and more important role in the field of electronics. As large server farms are developed to hold the hundreds of millions of terabytes of data circulating the internet, the need to condense all the data into energy efficient servers is increasing. As we come to the end of the “Moore’s Law” era of circuit capacitor and transistor density, the focus of the manufacturers is beginning to shift from outright storage capacity to refinements in read/write efficiency, and most importantly, lower power consumption.

Keywords- MIPS, bit-wise, bit-cell, MRAM, FPGA, TCR, DLC, Spintronic, efficient

I. Introduction

The MIPS program that is being executed is designed to search for the words “Knights” or “UCF” from a hard-coded paragraph in the program. The program first prompts the user to enter the word they would like to search for, the program then sorts through the user’s input to change every letter to uppercase. By every letter being uppercase the bit-wise value of the desired word can be more easily worked into a breaking loop function. The bit-wise values of the words “UCF” and “KNIGHTS” are 222 and 536 respectively. The value of the user’s altered input is then calculated and stored in register $t0. If the user wishes to search for the word “UCF” then the program directs to a set of branching loops designed to only search for word values of 222. If the user wishes to search for the word “KNIGHTS” then the program jumps to a set of branching loops designed to only search for words with a value of 536. The program then takes the hard-coded paragraph and begins to cycle through one bit at a time. The program adds each letter bit-by-bit until words of value 222 or 536 are reached. This is achieved by sequentially adding the bit-wise value of every letter until a space between words is reached. When a space is detected, the bit-wise value of the user’s input is compared to the sum of the bit-wise values of the last read word. Integrated into the loop that progresses the paragraph is an Index counter. The index counter increments the value of its designated register by one every time a space is detected. When the user’s desired word is detected within the paragraph the value of the index register is printed in the output box, thus displaying the index of every occurrence of the desired word. Once the program has completely processed every bit in the hard-coded paragraph, the program jumps to the main exit label. The number of occurrences of the desired word is printed in the output and the program is terminated.

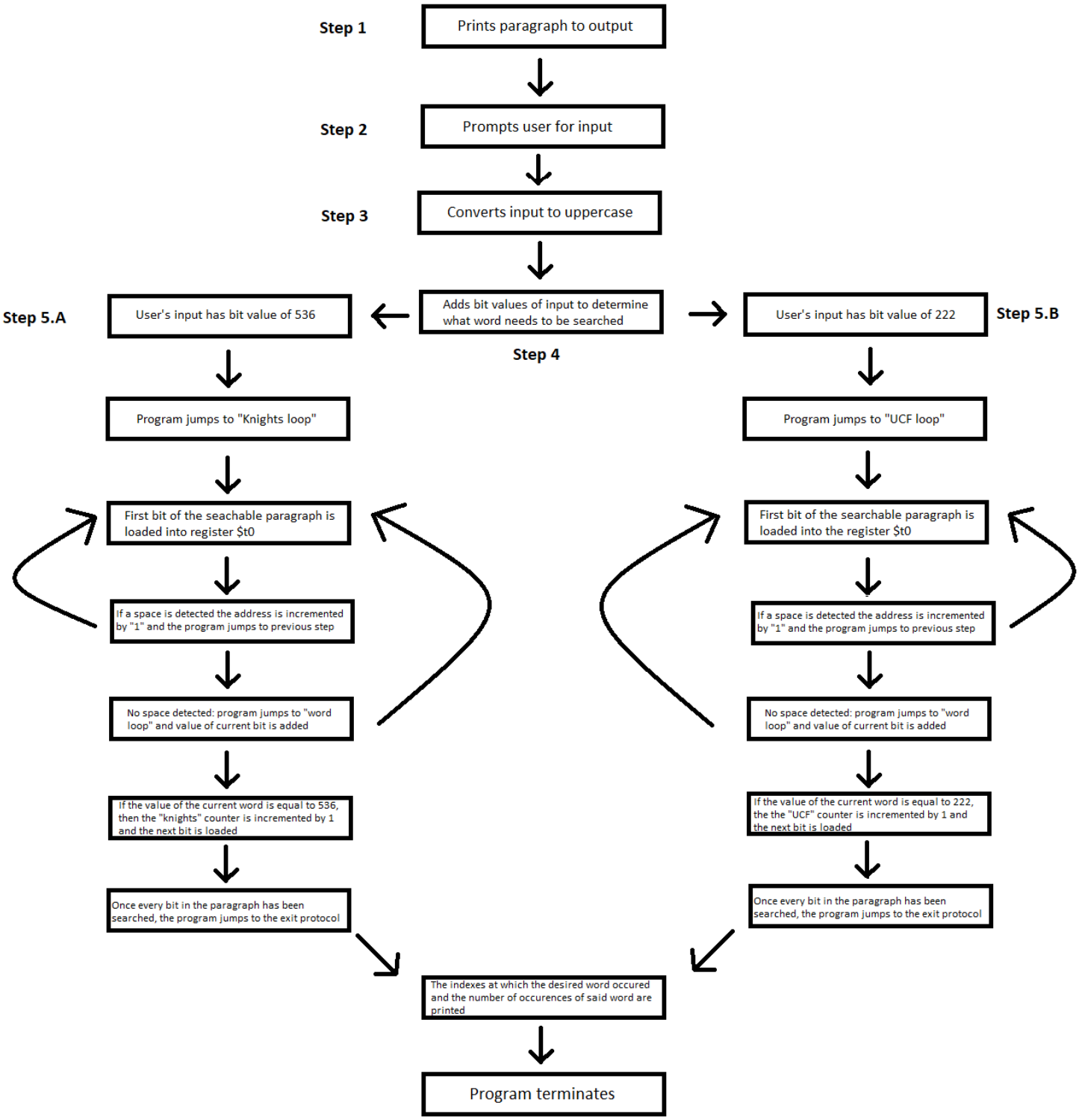

Figure 1: Flowchart of MIPS program

Disclosure- The program never fully ran as intended and would often loop infinitely without end. After many hours of troubleshooting and tinkering, no solution was found, and the program continues to loop indefinitely. To make up for the lack of data that could be gathered from broken MIPS code, all instruction statistics data for calculating energy usage were found by running the program for 5 seconds and then forcing the program to stop. The instruction counts and instruction statistics were then recorded and the calculations were performed.

II. Memory Bit-Cells

In a traditional memory cell, data is stored as bits (a 1 or a 0) in a semiconductor transistor called a MOSFET. When the semiconductor is fed an electric charge the data can be stored, read, or changed. Due to the nature of the transistor, once the charge is stored it requires very little energy to store the data. However, over time the charge from the semiconductor can begin to diminish, thus more electricity is required to keep it charged. MOSFET based memory is also volatile, meaning when power to the system is off, all the data stored in the semiconductors is lost.

More advanced modern forms of memory storage devices are trying to find more efficient means of storing data. One technology called *Spintronic* memory devices uses magnetic poles to influence the spin of a field of electrons thus inverting a magnetic torque onto electrodes in the circuit. The magnetic flux needed to polarize the electrons requires very little energy to create, and when power is cut from the system, the electrons maintain their magnetic polarities meaning Spintronic based memory is non-volatile.

III. Results and Discussion

Each of the memory technologies discussed in the previous section require different amounts of energy to perform their read functions. The purpose of this paper is to take the theoretical energy consumption for a read operation of each of these technologies and calculate how much energy it would take to run through the same MIPS program. The given read operation energy consumptions were as follows.

1. *Spintronic = 0.37 fj*
2. *Threshold Combinational Reduction (TCR) = 47.09 fj*
3. *Nanoscale Memory = 6.96 fj*
4. *Dynamic Latched Comparator (DLC) = 37.6 fj*

The MIPS program would then be run through with the *Instruction Statistic* tool enabled to ensure that the number of times each instruction is performed is calculated. However, as stated in the "*Disclosure"* section, the program was not able to run as intended. Thus, the program was ran for precisely 5.05 seconds and was then promptly stopped and the instruction counts were taken. The total energy consumed by the program is calculated by summing the products of "Energy per Instruction" and "Number of Operations" for each instruction type. The number of operations for each instruction type and their total energy consumptions are shown in *figure 2.*

Instruction Type	Number of Operations	Energy per Instruction	Total Energy Consumed
ALU	13972	2 fj	27.94 pj
Jump	6951	3 fj	20.85 pj
Branch	13908	4 fj	55.63 pj
Memory	6952	50 fj (write only)	347.6 pj
Other	17	6 fj	0.10 pj
Total Energy consumed w/o read operations			452.12 pj

Figure 2: Energy Usage by Instruction Data Type

To find the amount of energy each memory technology consumed for all the read operations in the duration of the MIPS program execution the read operation energy consumption for each of the technologies was multiplied by the number of memory operations in the program. The total read energies for each bit-cell type are given in *figure 3*.

Memory Type	Read operation Energy Consumption
Spintronic	(0.37 fj) × (6952) = 2.57 pj
TCR	(47.09 fj) × (6952) = 327.37 pj
Nanoscale	(6.96 fj) × (6952) = 48.46 pj
DLC	(37.6 fj) × (6952) = 261.40 pj

Figure 3: Read operation Energy Consumption by Memory Bit-cell Type

The values from *figure 3* where then used to calculate the total energy consumed while the MIPS program was run.

Memory Type	Total Energy Consumption
Spintronic	454.69 pj
TCR	779.49 pj
Nanoscale	500.58 pj
DLC	713.52 pj

Figure 4: Total Energy Consumption by Memory Bit-Cell Type

IV. Conclusion

As shown in *figure 3*, both Threshold Combinational Reduction and Dynamic Latched Comparator bit-cells have significantly higher energy consumption. The read operations alone for TCR and DLC account for 42% and 36.6% of the program's total energy consumption respectively. From these statistics Spintronic memory bit-cell technology is the most energy efficient as it uses nineteen times less energy than the next most efficient memory bit-cell type. Spintronic memory cell technology looks on paper to have the best performance-to-energy ratio of all the memory bit-cell technologies tested. Spintronic memory is extremely energy efficient and with its use in magnetic random-access memory (MRAM) it is still incredibly fast.

Five technical topics that I have taken away from this project are:

1. Current cutting-edge memory technology is slower at reading and writing than traditional CMOS memory, but their optimization in data density and energy consumption is a more desirable benefit.

2. Spintronic memory is nonvolatile because when power is lost it holds the last magnetic charge that was applied to it.

3. Photolithography is being used to develop hybrid nano/CMOS memory, but manufacturers are struggling to lower the defect rate due to the relatively new manufacturing process.

4. As technological advancements in memory density begin to slow, scientist and manufacturers have turned focus to optimizing memory efficiency rather than sheer capacity of storage devices.

5. A lot of research is being put into developing the flexibility of memory devices. Instead of having a fixed memory array developed for one specific task, manufacturers are looking to develop advanced FPGA devices that can be reprogrammed and reconfigured to meet the needs of the customer.

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