Improved energy expenditures by implementing Full Adder Boolean logic

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***Abstract*— In the field of computing we are always striving to create more efficient ways to solve certain issues that arise in time. As the world continues to advance in technology, we often see that the amount of processing power and efficiency are a major role in how we evolve as a planet. In this paper we look at the full adder and how it shown to be more efficient with the consumption of power. Even a small 20% reduction in energy consumption can be huge. The Full-Adder has shown to be more reliable as well.**

Keywords—Full Adder, FPGA, ALU, MFA, MTGB, RTM, STT, MIPS

I. Introduction

In the MIPS code provided the objective was to search a string that varied in length and find certain words provided by the user. After the program would output the number of occurrences and the index of the word found.

A. Project Design

In my program what I would do is begin by having a hard coded string that was provided and then we would ask the user for the two different words that he wanted to search for and then it would store those two words in a string. Then we would go through the entire string checking each character index checking if it was the same char. Then I would make it lower case for simplicity reasons and do a branch if equal to the character. Then do this process throughout the entire word and adding a one to the word counter if true. If the following code made it to the end of the word it would then branch to a another label and then have a predetermined array and move the index counter into it, then increment the array index value.

B. Test Cases

Test cases used in this laboratory were already pre-determined and given to us, but the code written would be valid for any string given to us and any two words entered by the user. We were given a string speaking of Knight scholarships and asked to search the occurrences of the word “Knight” & “UCF” since we attend the university.

Fig.1: Flowchart of the assembly program.

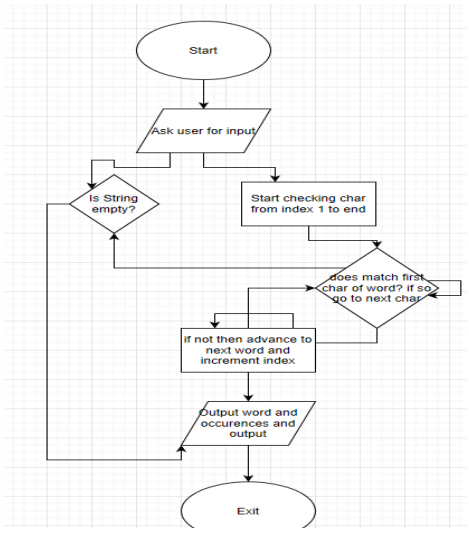

Fig.2: Sample outputs of the assembly program.

```
mylongstring: .asciiz "The Knights Graduation and Grant Initiat
# Prompt
# The Knights Graduation and Grant Initiative is a UCF award to
# to finish their degree. The Knights Success Grant is the most
# you need to be referred but it does not mean that all student
# submit a required application and complete the Knights Succes
```

```
# Please type in a word (up to 10 characters) that you ar
knight
# Please type in a second word (up to 10 characters) that
ucf
KNIGHT:   6
UCF:   2
```

```
# Please type in a second word (up to 10 char
night
THE:   16
NIGHT:   6
```

II. Full-Adder Circuit

In the contents of the full adder it consists of a a few logic gates implemented together to create a full adder. What the full adder does is receives three one-bit binary numbers. Which are the two numbers that operations are to be carried out on, then following it will consist of a carry bit. Which are regularly referred to as A , B , and Carry in. Once the full adder has received such information it will perform a calculation and out put only two different pieces of information. One being the sum of the two operands and following it will be the carry out bit.

In the following articles, there is data shown that the use of the full adder has many benefits when put against other forms of computing approaches. In the first article written by Ronald F. DeMara he showed that the use of the full adder had significant speed increases and substantially less energy consumption. In his study he achieved a 2-3.8-fold decrease in power dissipation and a 2.3- and 1.13-fold decreased delay on 1GHz and 500MGz operating speeds. Similar results are described in the article "Domain wall motion based magnetic adder" where they explain that area efficiency can be significantly increased, roughly 13-fold which is a major jump in any statistic. In a other article they explain through analysis that the MTGB-based ternary full adders compared to other circuits are the further reasonable circuit with lower thermal power expenditures.

Table I: Energy consumption for a single ALU Instruction in the designs provided in [1-3].

Design	Energy Consumption For Each ALU Instruction
[1]	0.6 pJ
[2]	6.3 pJ
RTM-based [3]	1.67 pJ
STT-based [3]	1.61 pJ

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
[1]	4.04993e-7J
[2]	4.85e-7J
RTM-based [3]	4.20e-7J
STT-based [3]	4.20e-7J

III. Results and Discussion

1) *ALU = Refer to Table I*
2) *Branch = 4 pJ*
3) *Jump = 3 pJ*
4) *Memory = 100 p*
5) *Other = 5 pJ*

Energy = (ALU * [1]) + (Branch * 4pJ) + (Jump * 3pJ) + (Memory * 100pJ) + (Other * 5pJ)

IV. Conclusion

To conclude the Full Adder has shown many benefits that are appealing to very large-scale corporations and even small ones. The full adder is a simple circuit when compared to other circuits and its advantages are necessary to push forward the evolution of technology as we become smarter and more efficient. The full adder has shown significant power reduction, allowing big scale corporations to reduce costs. Following power reduction strategies, it has also shown major improvements in performance. With the performance there has also been more signs of reliability in these circuits. To conclude the Full-Adder are very powerful and cost efficient circuits.

References

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