Latch Design Techniques used to Improve Reliability and Increase Efficiency of Memory Bit-Cells

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***Abstract*—**In this paper, reliability issues are granted through exposure of memory-bit cells and techniques built around Triple Modular Redundancy. The issue is not whether they work, but how to improve methods from different latches or schemes. Other topics bring up performance issues and reliability with SRAMS, etc. The project being tested takes user inputs of words and compares them to sentence where decimal values will be returned representing the number of cases of the words and their indexes. Results are granted from two specific words in each test, but with case sensitivity changing each time. The energy consumption is 707.28 fJ for the DNU-Latch.

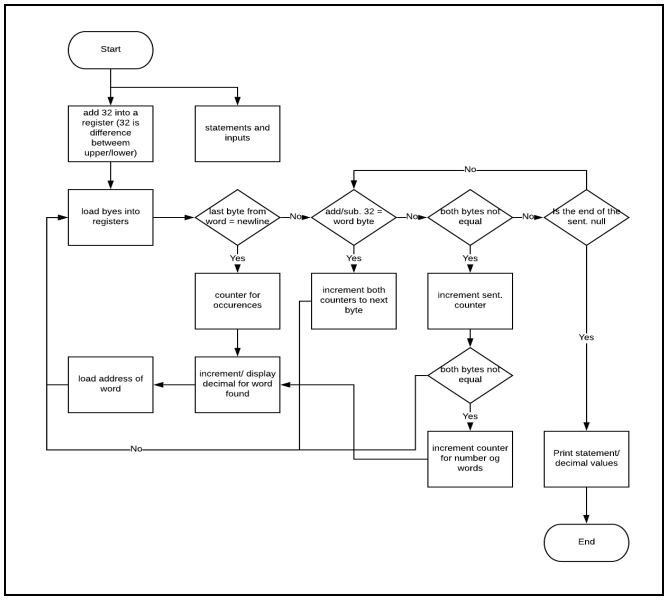
***Keywords*—**DICE-Latch, TMR, SRAM, Flash Cells, Static, DRAM, Reliability, and Floating Gate.

I. Introduction

The program takes an input given as a string and takes the users inputs of two words and finds the number of occurrences for each word in the string. As a whole, the bytes for the string and inputs are taken in one at a time and compared to each other to determine if one or two registers are incremented.

A. Project Design

The program first asks the user to input two words. The first half of the program searches for cases of the first word. The string and word are loaded into registers before the first loop. The loop starts with loading the first bytes into new registers, where the first cases check to see whether either the string or word reached its end. If it's the word, that means the word was found in the string, so branch to increment. If string, the program prints the statements. What's important is not being case sensitive. The difference between an uppercase character from its lowercase is a 32-decimal value from ascii table. The byte from the string is also loaded into two additional registers, where 32 will be either subtracted or added, and then compared to the byte from the word. In any case if the two bytes are equal, there is a branch to increment to the next byte. For the case there not equal, only the string will load the next byte. The jump from the next byte or increment will load the word into its register again. Each time two bytes are not equal, a space is checked between each word and if so, a counter represents the index of the word.



B. Test Cases

The inputs to the program include two words of varying length of up to ten characters that are not case sensitive. The purpose is to have varying case sensitives of the words to determine if the program recognizes each letter in the given sentence without being strictly case sensitive. Essentially, a character being uppercase in the input will match with the all the cases of upper/lower case in the string.

```
Enter a word: ucf
Enter another word: knight
The indexes at which your first word appear is: 1 19 59
The number of occureneces for your first word are: 3
The indexes at which your second word appear is: 27 29 42 75 96 100
The number of occureneces for your second word are: 6
-- program is finished running --

Enter a word: UCF
Enter another word: KNIGHT
The indexes at which your first word appear is: 1 19 59
The number of occureneces for your first word are: 3
The indexes at which your second word appear is: 27 29 42 75 96 100
The number of occureneces for your second word are: 6
-- program is finished running --
 Enter a word: uCF
 Enter another word: KNIghT
 The indexes at which your first word appear is: 1 19 59
 The number of occureneces for your first word are: 3
 The indexes at which your second word appear is: 27 29 42 75 96 100
 The number of occureneces for your second word are: 6
 -- program is finished running --
```

II. Memory Bit-Cells

The idea behind Triple Modular Redundancy acts as a voting circuit, where there are three gates and if one of them fails, the other two make the majority decision. In the case where the decision gate fails, the voters are then voting for each stage of the logic sequence, so there are no failure points.

Reliability techniques such as an Inherent Voter Based Scheme, uses majority voting where an inverter gate is used to rid the centralized voter block. “Bad Rows” take upon more than one defect in a row and TMR is then applied to the rows with either less defects or the number of “Bad Rows”.

Another design uses a DICE latch, where there are two cross-coupled latches. With two pairs of nodes, there may be a random pulse affecting the values, but there are additional nodes that “hold” the values without change. There also could be a particle strike of the unaffected nodes, but quickly reverse the effect by a transistor feeding the “hold” values in. With this, two cases exist, where immunity is granted from the “hold” nodes and the two affected nodes are not subsequent, so the “hold” values cannot be carried over.

SRAMs tend to degrade in performance over-time with a decline in stability due to factors ranging from changes in temperature to static stress [4]. The study of DDRSDRAM modules of different progressions went through stress tests such as changes in temperature and voltage level. With different distributions, observations realized show how current increase and voltage are accelerated from smaller technology [5]. With studies in automotive applications, embedded flash cells are studied in terms of its life cycle, where floating gate devices are studied in terms of production [6].

Table I: Energy consumption for a single bit-cell memory in the designs provided in [1-3].

Design	Energy consumption of a Single Bit-Cell Memory
SEU-Latch	0.88 fJ
DNU-Latch	0.28 fJ
NRAM	6.96 fJ
SEU Tolerant	1.51 fJ

III. Results and Discussion

1) *ALU =7784 fJ*
2) *Branch = 25,869 fJ*
3) *Jump = 2,540 fJ*
4) *Memory = Refer to Table I*
5) *Other = 12,845 fJ*

Table II: Total Energy consumption for the assembly program using designs provided in [1-3].

Design	Total Energy Consumption
SEU-Latch	2,222.88 fJ
DNU-Latch	707.28 fJ
NRAM	17,580.96 fJ
SEU Tolerant	3,814.26 fJ

The different designs used can be seen in Table II with their respective energy consumption. For each bit-cell, the energy can be seen in Table I for each design. As with the program used, the DNU-Latch clearly uses the least amount of energy granting greater efficiency and reliability in the long term. The NRAM uses the most energy by far which could result in a greater chance in failure if too much stress is applied. Each latch though is unique and needs to be used for the appropriate task.

IV. Conclusion

With memory bit-cells, many designs are created for specific tasks with some being more efficient than others. In this paper, the DNU-Latch resulted in the best design with the least amount of energy being consumed. Topics such as embedded flash cells, TMR, SRAM, DICE latch, and “Bad Rows”. The objective will remain to continue developing new techniques encompassing the best reliability.

References

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