Mousam Hossain

CONTACT

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EDUCATION

Ph.D. Candidate, Computer Engineering
GPA - **4.0/4/0** **August 2019- Present**
University of Central Florida, Orlando, FL,
US Advisor: **Dr. Ronald F. DeMara**

M.S. Electrical and Computer Engineering

August 2017- July 2019

GPA- **4.0/4.0**
North Dakota State University (NDSU), Fargo, ND, US
Advisors: **Dr. Sudarshan K. Srinivasan and Dr. Scott C. Smith**
Research focus: Asynchronous circuit design, Formal verification and advanced digital systems.
Dissertation: *Formal Verification Methodology for Asynchronous Sleep Convention Logic (SCL) circuits based on equivalence verification.* Consisted of developing:

- A fast and scalable verification methodology for SCL circuits based on equivalence checking, which ensures both safety and liveness.

B.Tech. Electronics and Communication Engineering **August 2009- June 2013**
GPA- **8.95/10**
Inst. Of Engineering & Management (IEM), West Bengal University of Technology (WBUT), Kolkata, WB, India.
Advisor: Dr. Malay Ganguly (Professor, H.O.D, ECE Dept.)
Senior Design Project: *Optimization of the performance of Microstrip Patch Antenna (MPA) using Particle Swarm Optimization (PSO) Algorithm /IE3D*

RESEARCH EXPERIENCE

Graduate Research, Computer Architecture Lab, UCF **Aug 2019 – Present**

- Conducting research on spintronics based emerging logic device circuits used in Computer Architecture.
- Conducting research on ARO project Edge-based Machine Intelligence for In-situ Video Processing using Binarized Neural Networks.

Graduate Research, Advanced Digital Design and Verification Lab, NDSU **Aug 2017 – May 2019**

- Conducting research for a project on formal verification of Quasi-Delay Insensitive (QDI) asynchronous circuits **funded** by National Science Foundation (NSF)**.**
- Developed first-ever formal verification methodology for Sleep Convention Logic (SCL) QDI asynchronous Circuits. Developed a verification methodology and verified numerous benchmarks by testing bugs during circuit synthesis. Used Python, SMT-LIB language, Z3 SAT solvers.

Undergraduate Research Assistant, Dept. of Electronics & Communication Engineering, IEM, India **2012-2013**

- Worked with the Electromagnetics and Antenna Design group of the dept. of Electronics and Communication Engineering at IEM, Kolkata, India.
- Focused on the optimization of antenna parameters to improve the performance of Microstrip Patch Antennas based on Particle Swarm Optimization (PSO) Algorithm.

TECHNICAL INTEREST

Beyond CMOS Computing, Reconfigurable and Evolvable Hardware, neural networks, High performance Computer Architecture, Asynchronous Logic, Low- Power Designs, Digital Design, and Advanced Digital Design.

PUBLICATIONS AND PRESENTATIONS

1. **Refereed Journal Article: M. Hossain**, A. Tatulian, S. Sheikhfaal, H. R. Thummala and R. F. DeMara, "Scalable Reasoning and Sensing Using Processing-In-Memory With Hybrid Spin/CMOS-Based Analog/Digital Blocks," in *IEEE Transactions on Emerging Topics in Computing*, 2022, doi: 10.1109/TETC.2022.3212341.
2. **Refereed Journal Article:** M. Liu, P. Borulkar, **M. Hossain**, R. F. Demara and Y. Bai, "Spin-Orbit Torque Neuromorphic Fabrics for Low-Leakage Reconfigurable In-Memory Computation," in *IEEE Transactions on Electron Devices*, vol. 69, no. 4, pp. 1727-1735, April 2022, doi: 10.1109/TED.2021.3140040.
3. **Refereed Technical Conference: M. Hossain**, A. Tatulian, H. R. Thummala, R. F. DeMara and S. Salehi, "Energy-/ Area-Efficient Spintronic ANN-based Digit Recognition via Progressive Modular Redundancy", in 55th proc. IEEE International Symposium of Circuits and Systems (ISCAS), 2023, Monterey, California. **(accepted)**
4. **Refereed Technical Conference:** R. Yarnell, **M. Hossain**, R. F. DeMara and Y. Bai, "Image Quantization Tradeoffs in a YOLO-based FPGA Accelerator Framework", in IEEE International Symposium on Quality Electronic Design (ISQED) 2023. **(accepted)**
5. **Refereed Technical Conference: M. Hossain,** S. Salehi, D. Mulvaney, and R.F. DeMara, "Embedded STT-MRAM Energy Analysis for Intermittent Applications using Mean Standby Duration", in proc. IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2021, (pp. 1-6).
6. **Refereed Technical Conference:** M. Liu, K. Han, S. Luo, M. Pan, **M. Hossain**, B. Yuan, R. F. DeMara , and Y. Bai, "An efficient Video Prediction Recurrent Neural Network using Focal Loss and Decomposed Tensor Train for Imbalance Dataset," in proc. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2021, Association for Computing Machinery, New York, NY, USA, 391–396. https://doi.org/10.1145/3453688.3461748.
7. **Refereed Technical Conference:** D. Crumley, **M. Hossain**, K. Martin, F. Ivey, R. F. DeMara, and Y. Bai, "Rehosting YOLOv2 Framework for Reconfigurable Fabric-based Acceleration", *IEEE SoutheastCon*, Mar. 2022 Mobile, AL, USA, 2022, pp. 445-446, doi: 10.1109/SoutheastCon48659.2022.9763979.
8. **Refereed Technical Conference: M. Hossain,** A. A. Sakib, S. K. Srinivasan and S. C. Smith, "An Equivalence Verification Methodology for Asynchronous Sleep Convention Logic Circuits," in proc. IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 2019, pp. 1-5.
9. **Poster presentation: M. Hossain,** R. F. DeMara, "Spin Based Embedded MRAM for Intermittently Powered Applications", at IEEE Design Automation Conference, (DAC) Young Fellows Program, 2021.
10. **Educational publication:** R. F. DeMara, S. Silvermann, M. Reddy-Vangala, and **M. Hossain**, "Imparting Future Workforce Skills using Virtualized Active Learning: A Case Study in an Engineering Core Course," *Florida Online Innovation Summit(FOIS-2020)*, Orlando, FL, USA, March 3, 2020.
11. **Invited talk:** Women in Research, North Dakota State University, Mar. 2019.

SKILLS

Languages: Verilog, VHDL, Python, Satisfiability Modulo Theories Library Language (SMT-LIB), Java, C, Assembly.
Formal Verification: Equivalence checking, Z3 SMT Solver.
Application Tools & Software: HSPICE, Xilinx Vivado, Vitis AI, Quartus II, ModelSim, MATLAB, Cadence Virtuoso (DRC, LVS).
Hardware Packages: FPGA (ALTERA DE2 series), Xilinx Basys3
Languages: Verilog, VHDL, Python, Satisfiability Modulo Theories Library Language (SMT-LIB), Java, C, Assembly.
Formal Verification: Equivalence checking, Z3 SMT Solver.
Application Tools & Software: HSPICE, Xilinx Vivado, Quartus II, ModelSim, MATLAB, Cadence Virtuoso (DRC, LVS).
Hardware Packages: FPGA (ALTERA DE2 series), Xilinx Basys3.

RELATED GRADUATE-LEVEL COURSEWORK

Future Computing Systems, Emerging Devices Computer Architecture, FPGA Design, Advanced Digital Design, Computer Architecture, Advanced Topics in Microelectronics, Low power Circuits and Systems design, Introduction to Lab-on-a-chip Technology, Introduction to Semiconductor devices, VLSI Design.

COURSEWORK RELATED PROJECTS

1. FPGA Design (EEE 5722C): **Implementing a RISC-V pipelined Processor** – Implementing pipeline in a RISC-V open source code, analyzing its impact on throughput efficiency and optimizing the pipeline throughput.
2. Computer Architecture (ECE 474/774): **Tomasulo's algorithm Simulator** - Developing a simple simulator in C++ to demonstrate Tomasulo's algorithm in a processor capable of performing basic integer arithmetic operations. The processor restraints were pre-specified such as the number of Reservation Stations, number of entries in Register Alias table, computational units, cycles of executions for each arithmetic operation etc.
3. Computer Architecture (ECE 474/774): **Tomasulo's algorithm with Re-Order Buffer implementation –** Extending the previous project to make the processor capable of handling divide by zero exceptions.
4. Advanced Digital Design (ECE 475/773) **NCL 2's Complement MAC** designed in VHDL. Testing it using exhaustive testbench and simulation macro.

TEACHING EXPERIENCE

Substitute Instruction: **Oct 2019, Nov 2021**

- Taught required core undergraduate lecture course **EEL3801**: Computer Organization during the Professor's absence during business travel. Was responsible for lecturing content, problem-solving, and answering questions.

Teaching Assistant, University of Central Florida **2019-Present**

- Guiding students on Assembly Language Programming using MARS Simulator, Verilog Coding by using design and simulation tools such as Xilinx Vivado and Basys3 FPGA board.
- Updating laboratory assignments and experiments, assisting students in the laboratory, and grading.
- **Courses taught** (SpS- Spring Semester, FS- Fall Semester, SS- Summer Semester)**:**
    I. **EEL 3801** - **Computer Organization**- **FS'19 to SpS'22**; Topics covered: Assembly language coding, syscalls, loops, dynamic instruction count optimization strategies, cache efficiency,MARS simulator tool debugging etc.

Teaching Assistant, North Dakota State University **2017-2019**

- Guiding students on FPGA Architecture and Programming, RTL simulation, Gate-Level Circuit Design, Transistor-Level Circuit Design, and VHDL Coding by using design and simulation tools such as Quartus and ModelSim.
- Updating laboratory assignments and experiments, assisting students in the laboratory, and grading.
- **Courses taught** (SS- Spring Semester, FS- Fall Semester)**:**
    I. ECE 374 - **Computer Organization**- SS'19, SS'18; Topics covered: R-type/I-type instructions, pipelines, processor design, FPGA implementations, VHDL, Hazards etc.
    II. ECE 475/773 - **Advanced Digital Design**, SS'19; Topics covered: FPGA implementations, ASM, FSM, Asynchronous Logic, VHDL etc.
    III. ECE 275 - **Digital Design**- FS'17, FS'18; Topics covered: FPGA implementations, VHDL, Combinational & Sequential circuits, Boolean simplifications, Counters etc.
    IV. ECE 376 - **Embedded Systems** - SS'18; Topics covered: Assembly programming, stepper motors, interrupts, TIMER interrupts etc.

Tutor, GTA, Electronic and Proficiency Center, (EPC) UCF **2019-2020**

- Conducted score clarification on exams and quizzes on multiple topics on Computer Organization (EEL 3801).
- Assisted students with better understand critical concepts, solving example problems to clarify doubts, and providing guidelines for their class projects.

Tutor, IEEE Eta-Kappa-Nu, NDSU **2018-2019**

- Lectured on multiple topics on Computer Organization, Computer Architecture, Digital Design, Advanced Digital Design; organized by the gamma Tau Chapter of IEEE-HKN at NDSU.
- Assisted students with better understand critical concepts, solving example problems to clarify doubts, and providing guidelines for their class projects.

WORK EXPERIENCE

Associate (Programmer), Cognizant Technology Solutions Corporation (CTS), India **Dec 2013- May 2017**
Clients: (Banking and Financial Services)

- F**use box Maintenance App-** The back-office application of a major credit card processor and merchant acquirer inthe USA. Provided highly successful deliverables for defects and enhancements.

  Projects:
  1. **Intelligent defaulting system in Online Case Management module- (Role: Module Lead, Programmer):** Implementation of an intelligent defaulting system to auto-populate data satisfying all the complex business rules of the client by a set of defaulting rules set up in the database. This innovation reduced typing effort, time and manual mistakes to a remarkable extent while filling online forms.
  2. **GWT Migration project (Role: Programmer)**- Successfully delivered migration of software application from licensed software GXT to open source GWT (Google Web Toolkit). All the components of GXT were custom made into GWT with a plethora of added features.
  3. **JBOSS Migration project (Role: Programmer) –** Successfully delivered migration of software application from licensed Tomcat to open-sourced JBOSS application server resulting in cost saving for client. Maven was used as the new build tool for project instead of Apache ANT.

- **First Data**
  Projects worked on: (Role: Team Member)
  Cross Site Request Forgery protection – Worked on the security of User Admin, Funding and Settlement Management, Rewards website modules based on issues reported by Fortify and Secure Assist tools such as dead codes/SQL injections/Password leaks etc.

INDUSTRIAL TRAINING

Trainee, Centre for Electronics and Test Engineers (CETE), Ministry of IT, Govt. of West Bengal, India **Dec'12- Jan'13**

- Received training on different microcontrollers and microprocessors, coding in assembly language, and finishing different projects based on microcontrollers.
- Final Project: *An intelligent, real-time Traffic Control System based on Microcontrollers*.

Trainee, Circle Telecom Training Centre (CTTC), Bharat Sanchar Nigam Limited, Govt. of India **Dec'11- Jan'12**

- Received training on different telecommunication technologies, fiber-optic communication, information encoding decoding techniques, mobile communications.
- Field study: Live telecommunication equipment deployed at BSNL headquarters, West Bengal Branch.

COMMUNITY SERVICES

- **Sales Coordinator, Distressed Children and Infants International (DCI),** North Dakota Chapter **2017-Present**
  - Being a part of the leadership group and successfully organizing multiple fundraising events;

- **Volunteer,** Science Olympiad, North Dakota **2018**

AWARDS AND HONORS

- Recipient of the **Design Automation Conference (DAC) Young Fellows,** 2021, including travel grant worth **$700**.
- **Winner** of **Best Research Video Award** at **Design Automation Conference (DAC) Young Fellow** 2021 worth **$100**.
- Recipient of the **Award for Excellence in Graduate Student Teaching,** Department of *CECS,* University of Central Florida, 2021.
- Recipient of **Danny Craig Scholarship** at UCF for community involvement with prize money of **$1000**, March 2021.
- Recipient of the **Electronic and Proficiency Center Best Tutor Award,** UCF, Fall 2019.
- Graduate Teaching Assistantship, Dept. of Electrical and Computer Engineering, NDSU (2017-2019).
- West Bengal Board of Secondary Education Scholarship for outstanding result, Govt. of West Bengal, India, 2006.

PROFESSIONAL AFFILIATIONS

- **President**, **Student Laureates of STEM Teaching and Learning** (SLSTL) Registered Student Organization at the University of Central Florida from Fall 2020- present.
- **Vice-President, Computer Hardware Innovation and Design Association** (CHIDA) Registered Student Organization at theUniversity of Central Florida from Spring 2021- present.
- **Phi-kappa-Phi Honor society,** since Aug 2021.
- **Tau Beta Pi,** FL-Delta chapter, since Fall 2020.
- **IEEE- Eta Kappa Nu**: Electrical and Computer Engineering Honor Society, since Fall 2017.
- **Member,** The HONOR Society.
- **Student Member,** Institute of Electrical and Electronics Engineers (IEEE), since Fall 2017.